REMARKS AND ARGUMENTS

Rejection under 35 USC § 102

Claims 1-5, 11, 13-15 and 20-23 are rejected under 35 USC § 102(e) as being anticipated by Lee (U.S. Patent No.: 6,605,835 B2). Applicants respectfully disagree.

Lee describes a ferroelectric capacitor formed in a stack which includes a first portion of an upper electrode, ferroelectric layer and lower electrode. Second portions of the upper electrode is electrically connected to the first portion of the upper electrode. The second portions cover the sidewalls of the capacitor stack but electrically isolated from the lower electrode by an insulating sidewall spacer. The second portion of the upper electrode serves as a hydrogen barrier layer to protect the ferroelectric layer of the stack.

Claim 1, as amended, recites an integrated circuit and method of fabricating an integrated circuit, respectively, having a feature formed on a substrate. A conductive radiation protection layer covers at least all portions of the feature which are sensitive to radiation damage. An insulating layer electrically isolates the radiation protection layer from the feature. Likewise, claim 20 recites a method for forming an integrated circuit in which a conductive radiation protection layer protects at least all portions of the feature which are sensitive to radiation damage and is electrically isolated from the feature by an insulating layer.

In rejecting the claims, the Examiner equates the second portions of the upper electrode of the ferroelectric capacitor with the radiation protection layer of claim 1. Even if this could be case, Applicants submit that Lee still fails to teach or suggest the invention as claimed. In particular, the second portions of the upper electrode in Lee are electrically coupled to the first portion of the upper electrode of the capacitor, not electrically isolated from the feature as

presently recited in claims 1 and 20. This is because in order for the second portions of the upper electrodes to serve as an effective barrier layer, they need to be connected to prevent any path for hydrogen to pass through. Therefore, Applicants submit the claims 1 and 20 are patentable over Lee. Since the remaining rejected claims are either directly or indirectly dependent on claim 1 or 20, these claims are also patentable.

Claim 1 is further rejected under 35 USC § 102(e) as being anticipated by Gnadinger (U.S. 2002/0153542 A1). Gnadinger discloses a 1 transistor (1T) memory cell which includes a gate stack and first and second diffusion regions on opposite first and second sides of the gate stack. The gate stack includes 3 sequential layers. The bottom layer is an interfacial layer, the intermediate layer is a ferroelectric layer and the top layer is a gate electrode layer. *See* Gnadinger, Fig. 2A, elements 31, 30 and 50. First and second conductive contacts which are electrically coupled to respective first and second diffusion regions are provided. *See* Gnadinger, Fig. 2A (elements 70 and 71). The contacts are electrically isolated from the various layers of the gate stack by an insulating layer. *See* Gnadinger, Fig. 2A, element 60.

In rejecting the claims, the Examiner takes the position that the conductive contacts are equivalent to the radiation protection layer and that the contacts cover at least all portions of the feature (e.g., gate stack) which are sensitive to radiation to reduce radiation damage thereto. Applicants respectfully disagree.

The conductive contacts, as described in Gnadinger, are only located on first and second opposite sides of the gate stack. In the context of a gate stack, the edges of the various layers making up the gate stack are exposed on all sides of the gate stack. In the case of Gnadigner, the portions of the feature which are sensitive to radiation are the edges of the ferroelectric layer. Applicants submit that the contacts cannot completely surround the edges of the ferroelectric

layer. This is because the edges of the ferroelectric layer are exposed on all sides of the gate stack while the contacts only cover opposite sides of the gate stack. As such, the conductive contacts would leave at least some portions of the edges of the ferroelectric unprotected. Therefore, the conductive contacts do not cover at least all portions of the feature which are sensitive to radiation, as presently recited in claim 1.

In order for the conductive contacts to completely at least cover all portions of the gate stack, the conductive contacts would have to completely surround all sides of the gate stack. However, it is clear that if this were the case, the diffusion regions of the transistor would be shorted, thus rendering the memory cell inoperable. As such, the conductive contacts cannot and do not cover at least all portions of the feature which are sensitive to radiation, as recited by claim 1. Applicants therefore submit that claim 1 is patentable over Gnadinger and respectfully request the withdrawal of the rejection under 35 USC § 102(e) based on Gnadinger.

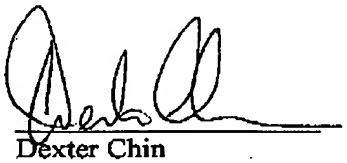
Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance and the issuance of a formal Notice of Allowance at an early date is respectfully requested.

Should the Examiner believe that a telephone conference would expedite prosecution of this application, please telephone the undersigned attorney at his number set out below.

Date: October 19, 2004

Respectfully submitted,



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